

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 16, line 2, please change "extend" to --extent--; and  
line 22, please change "at" to --out--.

IN THE CLAIMS:

Please cancel claims 7 and 8 without prejudice or disclaimer of subject matter.

Please amend claims 9, 10 and 14 as follows:

9. (Amended) An apparatus for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, comprising:

a processor;

memory connected to said processor;

said memory having instructions for said processor to

determine key pins for [each of said] identified hardware elements from a generic netlist;

extract critical design structure and hierarchy from the generic netlist;

apply bottom-up synthesis to modules and sub-modules of the IC design;

apply top-down characterization to modules and sub-modules of the IC

design;

Serial No.: 09/026,790

repeat said bottom-up and said top-down applications until constraints are satisfied; and

create design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.

10. (Amended) An apparatus for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, comprising:

al means for determining key pins for [each of said] identified hardware elements from a generic netlist;

means for extracting critical design structure and hierarchy from the generic netlist;

means for applying bottom-up synthesis to modules and sub-modules of the IC design;

means for applying top-down characterization to modules and sub-modules of the IC design;

means for repeating said bottom-up and said top-down applications until constraints are satisfied; and

means for creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.

---

14. (Amended) A computer system for generating synthesis scripts to synthesize integrated circuit (IC) designs in RTL level description into gate-level description, said system comprising:

means for determining key pins for [each of said] identified hardware elements from a generic netlist;

means for extracting critical design structure and hierarchy from the generic netlist;

means for applying bottom-up synthesis to modules and sub-modules of the IC design;

means for applying top-down characterization to modules and sub-modules of the IC design;

means for repeating said bottom-up and said top-down applications until constraints are satisfied; and

means for creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.

---

Please add claims 15 to 20 as follows:

---

--15. A method according to Claim 1, wherein input/output conditions and constraints of the modules of the IC design captured during the top-down characterization are used to re-optimize the IC design during the bottom-up synthesis.

16. A computer storage medium according to Claim 11, wherein input/output conditions and constraints of the modules of the IC design captured during the top-down characterization are used to re-optimize the IC design during the bottom-up synthesis.

17. A process according to Claim 13, wherein input/output conditions and constraints of the modules of the IC design captured during the top-down characterization are used to re-optimize the IC design during the bottom-up synthesis.

18. An apparatus according to Claim 9, wherein input/output conditions and constraints of the modules of the IC design captured during the top-down characterization are used to re-optimize the IC design during the bottom-up synthesis.

19. An apparatus according to Claim 10, wherein input/output conditions and constraints of the modules of the IC design captured during the top-down characterization are used to re-optimize the IC design during the bottom-up synthesis.

20. A computer system according to Claim 14, wherein input/output conditions and constraints of the modules of the IC design captured during the top-down characterization are used to re-optimize the IC design during the bottom-up synthesis.--

---